IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) An apparatus for controlling a physical layer interface of a network interface card in real time, said apparatus comprising:

a first memory capable of storing a multitasking control program, said multitasking control program comprising a main routine and a plurality of subroutines callable by said main routine;

a second memory capable of storing a plurality of multitasking vectors associated with said multitasking control program; and

a microcontroller capable of executing said multitasking control program; [[,]]

wherein program execution control is transferred from said main routine to a first one of said plurality of subroutines when said first subroutine is called by said main routine; and

wherein said first subroutine, upon encountering a decision point in said first subroutine that is not yet capable of being decided, updates a first one of said plurality of multitasking vectors associated with said first subroutine with an address of said decision point and transfers program execution control back to said main routine.

2. (Previously Presented) The apparatus as set forth in Claim 1 wherein said main routine uses said first multitasking vector to subsequently transfer program execution control back to said first subroutine at said address of said first decision point.

3. (Previously Presented) The apparatus as set forth in Claim 2 wherein said first memory comprises a read-only memory (ROM) associated with said microcontroller.

4. (Previously Presented) The apparatus as set forth in Claim 3 wherein said second memory comprises a random access memory (RAM) associated with said microcontroller.

5. (Previously Presented) The apparatus as set forth in Claim 4 wherein said ROM and said RAM are internal to said microcontroller.

6. (Previously Presented) The apparatus as set forth in Claim 4 wherein at least one of said ROM and said RAM comprises an external device coupled to said microcontroller.

7. (Previously Presented) The apparatus as set forth in Claim 2 wherein said first memory and said second memory comprise a random access memory (RAM) associated with said microcontroller.

8. (Previously Presented) The apparatus as set forth in Claim 7 wherein said RAM comprises an external device coupled to said microcontroller.

9. (Currently Amended) A processing system comprising:

a data processor; and

a network interface card for coupling said processing system to a data network, said network interface card comprising an apparatus for controlling a physical layer interface of said network interface card in real time, said apparatus comprising:

a first memory capable of storing a multitasking control program, said multitasking control program comprising a main routine and a plurality of subroutines callable by said main routine;

a second memory capable of storing a plurality of multitasking vectors associated with said multitasking control program; and

a microcontroller capable of executing said multitasking control program; [[,]]

wherein program execution control is transferred from said main routine to a first one of said plurality of subroutines when said first subroutine is called by said main routine; and

wherein said first subroutine, upon encountering a decision point in said first subroutine that is not yet capable of being decided, updates a first one of said plurality of multitasking vectors associated with said first subroutine with an address of said decision point and transfers program execution control back to said main routine.

10. (Previously Presented) The processing system as set forth in Claim 9 wherein said main routine uses said first multitasking vector to subsequently transfer program execution control back to said first subroutine at said address of said first decision point.

11. (Previously Presented) The processing system as set forth in Claim 10 wherein said first memory comprises a read-only memory (ROM) associated with said microcontroller.

12. (Previously Presented) The processing system as set forth in Claim 11 wherein said second memory comprises a random access memory (RAM) associated with said microcontroller.

13. (Previously Presented) The processing system as set forth in Claim 12 wherein said ROM and said RAM are internal to said microcontroller.

14. (Previously Presented) The processing system as set forth in Claim 12 wherein at least one of said ROM and said RAM comprises an external device coupled to said microcontroller.

15. (Previously Presented) The processing system as set forth in Claim 10 wherein said first memory and said second memory comprise a random access memory (RAM) associated with said microcontroller.

16. (Previously Presented) The processing system as set forth in Claim 15 wherein said RAM comprises an external device coupled to said microcontroller.

17. (Previously Presented) For use in a network interface card having a physical layer interface controllable by a microcontroller embedded therein, a method of operating the microcontroller comprising the steps of:

storing a multitasking control program, the multitasking control program comprising a main routine and a plurality of subroutines callable by the main routine;

storing a plurality of multitasking vectors associated with the multitasking control program; and

executing the multitasking control program in a microcontroller;

transferring program execution control from the main routine to a first one of the plurality of subroutines when the first subroutine is called by the main routine;

when the first subroutine encounters a decision point in the first subroutine that is not yet capable of being decided, updating a first one of the plurality of multitasking vectors associated with the first subroutine with an address of the decision point; and

transferring program execution control back to the main routine.

18. (Previously Presented) The method as set forth in Claim 17 further comprising the step of using the first multitasking vector to subsequently transfer program execution control from the main routine back to the first subroutine at the address of the first decision point.

19. (Previously Presented) The method as set forth in Claim 18 wherein the first memory comprises a read-only memory (ROM) associated with the microcontroller.

20. (Previously Presented) The method as set forth in Claim 19 wherein the second memory comprises a random access memory (RAM) associated with the microcontroller.

21. (Previously Presented) The method as set forth in Claim 20 wherein the ROM and the RAM are internal to the microcontroller.

22. (Previously Presented) The method as set forth in Claim 20 wherein at least one of the ROM and the RAM comprises an external device coupled to the microcontroller.